Manufacturable and Reliable Millimeter-Wave HJFET MMIC Technology Using Novel 0.15μm MoTiPtAu Gates

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ABSTRACT

This paper describes a manufacturable and reliable millimeter-wave heterojunction FET (HJFET) MMIC technology, in which a novel 0.15μm MoTiPtAu T-shaped gate has been successfully employed. Excellent DC and RF device characteristics, including *Imax* of ~600mA/mm, *BVgd* of >10V and *Fmax* of ~200GHz, were confirmed. High temperature DC-bias tests predict an MTTF of 1.5×10^7 hours at a channel temperature of 150°C. The 2-stage MMIC amplifier, fabricated using the developed technology, exhibited a 69.5mW output power with 14.4% power-added efficiency at 56GHz with good uniformity.

INTRODUCTION

Millimeter-wave MMIC modules are attracting considerable attention for future wireless system applications, including high-speed wireless LANs and image data transmissions. To put these applications to practical use, not only high performance but also good reliability and manufacturability are required for FETs comprising MMICs. Although much effort has been devoted to the development of high performance device technology [1-4], little attention has been paid to its reliability issues [5,6].

The purpose of this work is to develop a manufacturable and reliable HJFET technology for high volume commercial millimeter-wave MMIC applications.

DEVICE STRUCTURE

The schematic cross section of the fabricated device is shown in Fig. 1. Epitaxial layers were grown by MBE on a 3-inch semi-insulating GaAs substrate. The active part of the structure consists of an undoped $In_{0.2}Ga_{0.8}As$ channel layer sandwiched between two heavily doped n-type $Al_{0.22}Ga_{0.78}As$ layers. A 28nm undoped $Al_{0.22}Ga_{0.78}As$ layer was used as a Schottky contact layer. Devices with 0.15μm T-shaped gates were fabricated by electron-beam evaporation and lift-off technique employing direct-write electron-beam lithography [7]. Sequentially deposited gate metals consist of 10nm Mo, 20nm Ti, 20nm Pt, and 450nm Au. Figure 2 shows SEM cross section of the fabricated 0.15μm MoTiPtAu T-shaped gate. The Mo source temperature was carefully controlled during the Mo metallization step to ensure good reproducibility. All the devices were passivated with a 100nm-thick SiN film.

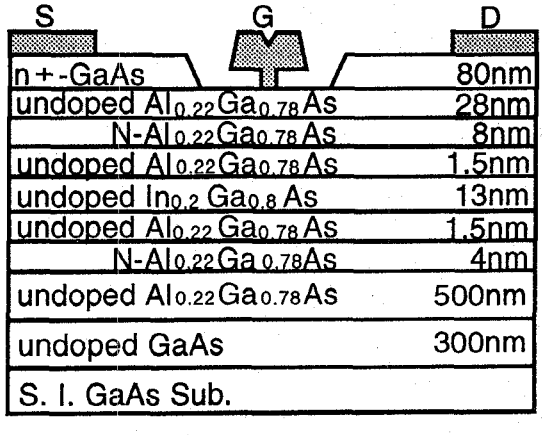

Fig. 1. Schematic cross section of fabricated HJFET

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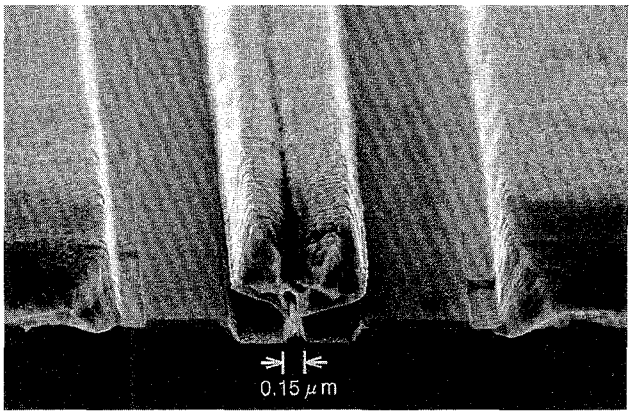

Fig. 2. 0.15μm T-shaped MoTiPtAu gate.

DEVICE CHARACTERISTICS

Typical DC drain I-V characteristics of the fabricated HJFET are shown in Fig. 3. Reflecting the electronic properties of the double-doped double heterostructure, a maximum drain current (*Imax*) of ~600mA/mm with rather a flat transconductance (*gm*) of ~400mS/mm was obtained at Vd=4V. A gate-to-drain breakdown voltage (*BVgd*) measured was more than 10V. The fairly high *BVgd* obtained is primarily due to the use of an undoped Schottky layer. Figure 4 illustrates the uniformity of saturation drain current (*Idss*) measured on a 3-inch diameter wafer. An average *Idss* and its standard deviation were measured to be 454mA/mm and 67mA/mm, respectively. Also the evaluated average *gm* of 410mS/mm and its standard deviation of 22mS/mm

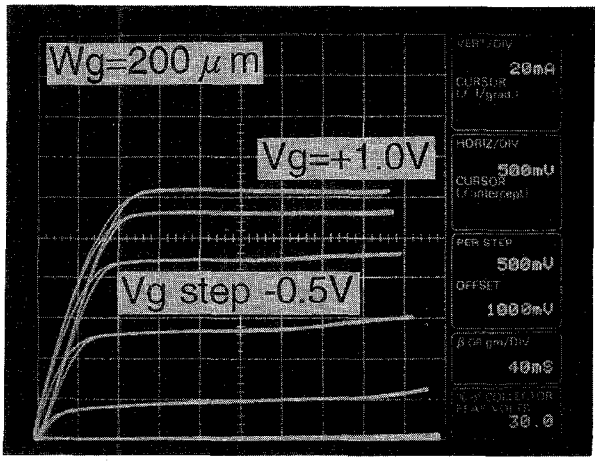

Fig. 3. DC drain I-V characteristics of a $0.15\times200\mu m^2$ MoTiPtAu gate HJFET.

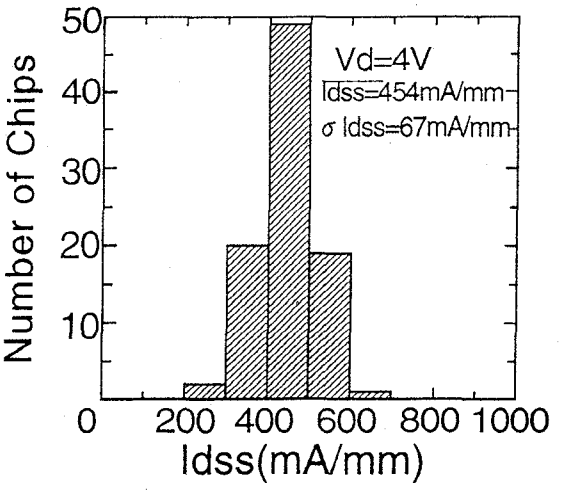

Fig. 4. Histogram of Idss for the MoTiPtAu gate HJFET on a 3-inch diameter wafer.

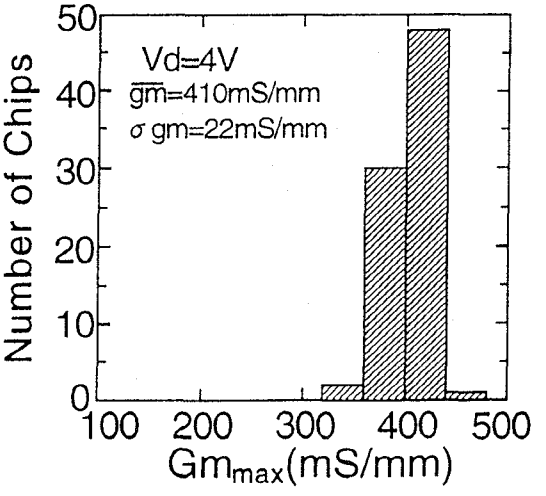

Fig. 5. Histogram of transconductance for the MoTiPtAu gate HJFET on a 3-inch diameter wafer.

were obtained (see Fig. 5). Similar uniformity in the device characteristics were confirmed over consecutive 4 lots (8 wafers/lot), indicating sufficient reproducibility of the developed MMIC technology employing a wet chemical recess etching technique. For all the wafers processed through 4 lots, the average *Imax* and *BVgd* evaluated on each wafer were distributed in the range of 540mA/mm to 610mA/mm and in the range of 10 to 14V, respectively.

S-parameter measurements were performed up to 60GHz for a Wg=100μm (50μm×2) device. Typical gain versus frequency plot, as illustrated in Fig. 6, indicates a power-gain cutoff frequency (*Fmax*) of 200GHz, including a maximum value of 223GHz. The current-gain cutoff frequency (*Ft*) was in the range of 55-65GHz.

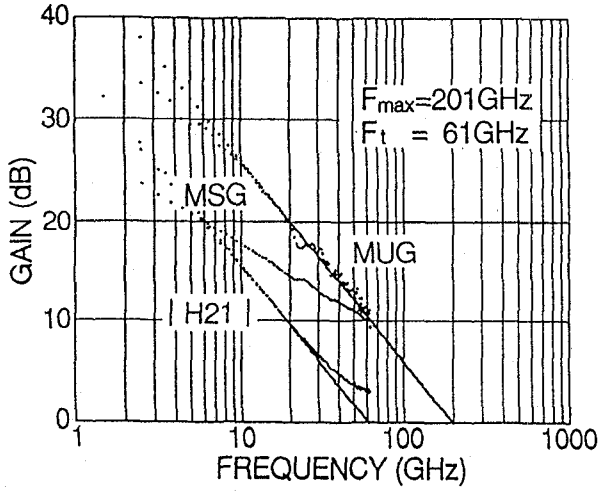

Fig. 6. Gain versus frequency for the MoTiPtAu 0.15μm HJFET.

RELIABILITY

High temperature storage tests were carried out to accelerate thermally-activated failure mechanisms. The results at an ambient temperature of 259°C are given in Fig. 7. The developed MoTiPtAu gate HJFET exhibited only a 5% change in *gm* after 2000 hours at 259°C, while the conventional TiPtAu HJFET showed a distinct onset of degradation after 850 hours. Also only a 8% change in *gm* was observed for the developed device at 295°C after 1450 hours. These results indicate that the interdiffusion between the barrier metal of Mo and the AlGaAs Schottky layer is negligibly small. High temperature DC-bias tests were also carried out. Figure 8 shows an arrhenius plot of the measured data. The median-time-to-failure (MTTF) values estimated at channel temperatures of 286 and 300°C suggested a projected life of 1.5×10^7 hours at a channel temperature of 150°C with an activation energy of 1.65eV. These reliability results obtained for the developed HJFETs are encouraging for a variety of MMIC applications.

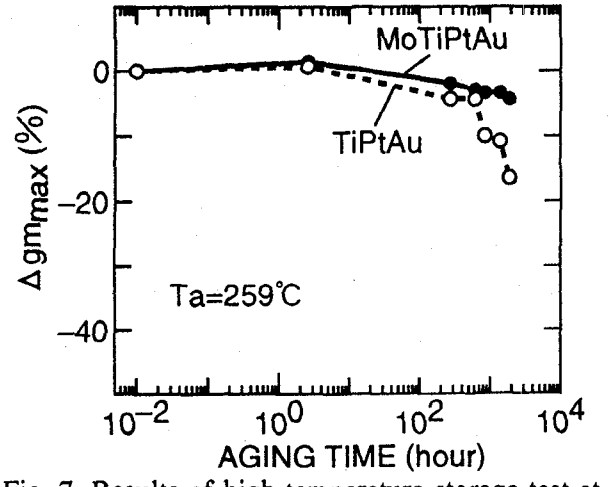

Fig. 7. Results of high-temperature storage test at 259°C.

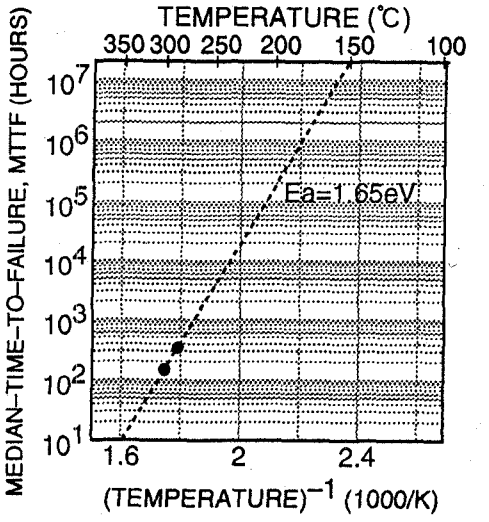

Fig. 8. Arrhenius plot of the measured data after high temperature DC-bias tests.

MMIC PERFORMANCE

To confirm the feasibility of our novel MMIC technology, two-stage MMIC amplifiers (100μm/200μm gate width) were fabricated. The amplifier has input and output matching circuits, DC-blocking MIM capacitors and gate and drain DC bias networks with a simple microstrip line configuration. Input and output matching circuits consist of transmission lines and open stubs. All groundings were made through via-holes of 30μm square. The chip size is $2.2\times2.2mm^2$.

At 56GHz, an average small-signal gain and its standard deviation of 15.41dB and 0.9dB, respectively, were obtained from 12 samples fabricated on a 3-inch wafer. This result ensures a good process uniformity of the present technology at millimeter-wave frequency (see Fig. 9). Millimeter-wave power performance was also evaluated. At 56GHz, a maximum output power of 69.5mW was measured with an associated gain of 6.72dB and 14.4% power-added efficiency (see Fig. 10).

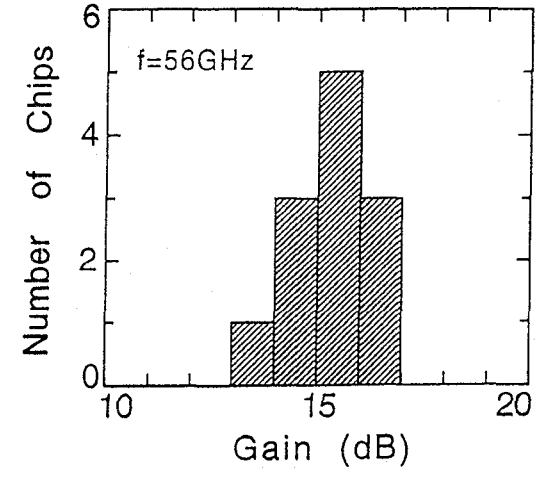

Fig. 9. Histogram of small-signal gain at 56GHz for 2-stage MMIC amplifier.

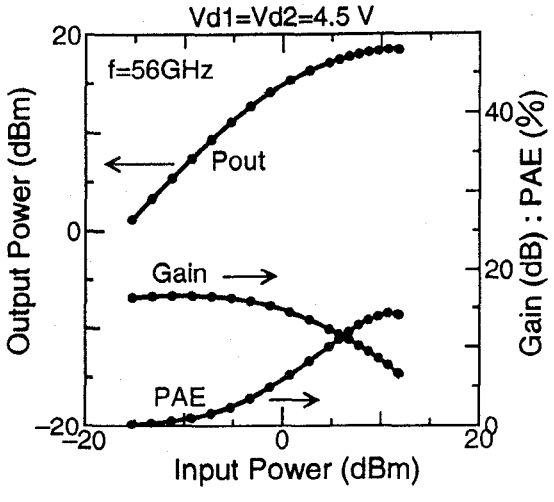

Fig. 10. Output power and power-added efficiency as a function of input power at 56GHz for 2-stage MMIC amplifier.

CONCLUSION

We have successfully developed a millimeter-wave HJFET MMIC technology using novel MoTiPtAu 0.15μm T-shaped gates. Good uniformity was confirmed by carefully controlling the evaporation conditions. The fabricated HJFET exhibited excellent DC and RF characteristics of *Imax*~600mA/mm, *BVgd*>10V and *Fmax*~200GHz. An MTTF of over 1.5×10^7 hours was projected at a channel temperature of 150°C. The power performance of the 2-stage MMIC amplifier exhibited a maximum output power of 69.5mW with 14.4% power-added efficiency. These results indicate that the present MoTiPtAu gate HJFET technology is promising for reproducible millimeter-wave MMIC applications with excellent reliability.

ACKNOWLEDGEMENTS

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REFERENCES

[1] P.M.Smith, P.C.Chao, L.F.Lester, R.P.Smith, R.R.Lee, D.W.Ferguson, A.A.Jabara, J.M.Ballingall, and H.H.G.Duh, "InGaAs Pseudomorphic HEMTs for Miilimeter Wave Power Applications," *IEEE MTT-S Digest*, pp.927-930, 1988.

[2] C.K.Pao, G.L.Lan, C.S.Wu, A.Igawa, M.Hu, J.C.Chen and Y.C.Shih, "V-Band High-Efficiency Monolithic Pseudomorphic HEMT Power Amplifiers," *IEEE Microwave and Guided Letters*, 2, pp.394-396, 1992.

[3] M.Funabashi, K.Hosoya, K.Ohata, K.Onda, N.Iwata and M.Kuzuhara, "High Gain V-Band Heterojunction FET MMIC Power Amplifiers," *Technical digest of GaAs IC Symposium*, pp.379-382, 1993.

[4] A.K.Sharma, G.Onak, R.Lai and K.L.Tan, "A High Power and High Efficiency Monolithic Power Amplifier at V-band Using Pseudomorphic HEMTs," *Digest paper of IEEE 1994 Microwave and Millimeter-Wave Monolithic Circuits Symposium*, pp.73-76, 1994.

[5] W.W.Hu, P.C.Chao, M.Y.Kao, P.Ho, R.J.Finke and A.W.Swanson, "Reliability of State-of-the-Art GaAs Pseudomorphic Low-Noise HEMTs," *Technical digest of GaAs IC Symposium*, pp.191-194, 1991.

[6] C.H.Chen, Y.Saito, H.C.Yen, K.Tan, G.Onak and Joe Mancini, "Reliability Study on Pseudomorphic InGaAs Power HEMT Devices at 60GHz," *IEEE MTT-S Digest*, pp.817-820, 1994.

[7] N.Samoto, Y.Makino, K.Onda, E.Mizuki and T.Itoh, "A Novel Electron-Beam Exposure Technique for 0.1μm T-shaped Gate Fabrication," *J. Vac. Sci. Technol.*, B8, pp.1335-1338, 1990.